12/20/99

UTILITY PATENT APPLICATION TRANSMITTAL

(for Noncontinuing, Nonprovisional Applications under 37 C.F.R. §1.53(b))

Attorney Docket No. 65611

Box PATENT APPLICATION
Commissioner of Patents and Trademarks
ATTENTION: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the nonprovisional, noncontinuing patent application for:

Title: METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

First Named Inventor or Application Identifier: Rajagopalan, et al.

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

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Date of Deposit December 16, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR §1.10 on the date indicated above and is addressed to the Asst. Commissioner for Patents and Trademarks, Washington, D.C. 20231.

Carrie Merzbacher
(Typed or printed name of person mailing)

(Signature of person mailing)

(X) 14 pages of the specification (including claims and cover sheet) are enclosed.

(X) 5 sheet(s) of drawings are enclosed. ( ) Formal ( ) Informal

(X) An executed Oath or Declaration and Power of Attorney naming the actual inventors is enclosed.

(X) An Assignment(s) of the invention to LSI Logic Corporation, and cover sheet are enclosed.

(X) A check in the amount of $ 40.00 to cover the fee for recording the assignment(s) is enclosed.

(X) A Return Receipt Postcard is enclosed (MPEP §503).

( ) Priority of application number ___/_____ filed on _____ in _____ is claimed under 35 U.S.C. §119.

( ) A certified copy of the priority document is enclosed.

( ) A MicroFiche Computer Program (Appendix) is enclosed.

( ) A Nucleotide and/or Amino Acid Sequence Submission is enclosed.

( ) A Computer Readable Copy is enclosed.

( ) A Paper Copy (Identical to Computer Copy) is enclosed.

( ) A Statement Verifying Identity of above Copies is enclosed.

(X) The filing fee is calculated below:

Fee Calculation For Claims As Filed

(a) Basic Fee					$ 760.00
(b) Independent Claims	3	- 3 =	0	x $ 78.00 =	$ 0
(c) Total Claims	11	- 20 =	0	x $ 18.00 =	$ 0
(d) Fee for Multiply Dependent Claims				$260.00	$

Total Filing Fee $ 760.00

( ) A Statement(s) of Status as Small Entity is enclosed, reducing the Filing Fee by half to: $

(X) A check in the amount of $ 760.00 to cover the filing fee is enclosed.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§1.16-1.17 during its entire pendency, or credit any overpayment, to Deposit Account No. 06-1135. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1135. This sheet is filed in duplicate.

(X) Address all future communications to:

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December 16, 1999

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Patent
Docket No. 65611
LSI-6653

PATENT APPLICATION

METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

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MINH VUONG

PATENT APPLICATION

METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

INVENTORS: SARATHY RAJAGOPALAN
MINH VUONG

TECHNICAL FIELD

The present invention relates to the use and construction of thermal profiling devices used in flip-chip semiconductor device fabrication. In particular, the present invention relates to a method and apparatus for obtaining an accurate thermal profile of a flip-chip during processing.

BACKGROUND OF THE INVENTION

The present invention relates to the field of so-called flip-chip packaging. Flip chip technology is well known in the art of semiconductor packaging and detailed information concerning flip chip packaging may be found in references such as Microchip Fabrication (3rd Ed.) by Van Zant, P., Chapter 18 "Packaging" (1997) and Ball Grid Array Technology, edited by Lau, John H. (1995) which are hereby incorporated by reference. Some methods of flip-chip packaging use packaging substrates which include one or more bonding pads on one of the substrate surfaces. These bonding pads have a number of circuit connections which will be contacted to a semiconductor chip (or "die"). The die features a plurality of leads which are used to interconnect the die to the packaging substrate. In order to efficiently connect the die to the bonding pad, the leads of the die are treated with tiny bumps of electrically conductive material (the bumps are typically formed of solder), which are used to interconnect the die to other circuit elements, including a bonding pad. Ordinarily, the dies are attached by dipping the die in flux such that the bump surfaces are covered in a small amount of flux. The flux treated die is then carefully aligned and placed on corresponding bonding pads of the packaging substrate. The packaging substrates are then placed in a reflow furnace, where the packaging substrate and die are subjected to a carefully controlled temperature process

designed to optimize the bond between the bumps and the bonding pad. This process of heating the bumps to desired melting temperature to electrically connect the die to the packaging substrate is known as reflow. Once this reflow process is completed, the packaging substrates and their newly bonded dies are subjected to further processing as needed.

In order to create a good contact between the die and the bonding pad, the process temperatures must be carefully controlled. A typical attachment process begins by aligning the die to the substrate and tacking it in place with flux. Then the die and packaging substrate are placed in a reflow furnace. For example, multizone reflow furnaces may be used to treat the die and package to the required temperatures. In the first zone the die and package are typically preheated to a baseline preheating temperature. Once preheated, the substrate and die are passed into a melt zone, typically a higher temperature. There the substrate and die are then subjected to a melt temperature which melts the solder bumps creating the bond between the bonding pad and the die. Once this is accomplished, the die and substrate are passed onto a cool down zone of the furnace, which allows the solder to cool without degrading the bond between the die and bonding pad. The temperature of each zone is largely dependent on the type of solder used to form the bumps. Each of these three steps (preheat, melt, and cool down) are very temperature critical requiring accurate thermal calibration of each zone. In the past, these temperatures were calibrated by a process known as thermal profiling. Thermal profiling is used to monitor a temperature vs. time curve. Although the reflow furnaces themselves are set at a certain temperature, this is not the same as the temperature at the interface between the die and the packaging substrate. Since it is the interface temperature that is critical, more accurate measurements of the interface temperature are required. Previously, thermal profiling had been done by placing a die on a packaging substrate, then attaching a thermocouple on top of the die and running the substrate through a preheat, melt, cool down cycle in a reflow furnace. The furnace temperatures were then adjusted until the optimum preheat, melt, and cool down temperatures were measured by the thermocouple.

The inventors have discovered that the thermal profile, using these methods does not accurately profile the temperature at the interface between the die and the packaging substrate. The inventors have discovered that the temperatures of the previously used methods can vary as much as 10° C from the actual interface temperature. This leads to sub-

optimal bonding of the solder bumps to the bonding pad. This increases chip failure rate and reduces chip reliability, and is therefore undesirable.

What is needed is a method and device for more accurately measuring the reflow temperatures at the interface between the die and the packaging substrate.

SUMMARY OF THE INVENTION

Accordingly, the principles of the present invention contemplate a method and device for accurately obtaining a thermal profile of a flip-chip die and packaging substrate.

In accordance with the principles of the present invention the present invention contemplates a device for obtaining an accurate thermal profile of semiconductor devices during processing, the invention comprising a packaging substrate, a semiconductor die, and a thermocouple, all being secured to together such that the thermocouple is positioned and secured at the interface between the substrate and the die.

Additionally, the principles of the present invention contemplate methods of constructing a devices of a type described above. Such methods comprising the steps of providing a semiconductor die and providing a packaging substrate, the substrate including a first side and a second side, said first side having a bonding pad for receiving the semiconductor die. A thermocouple is also provided. The thermocouple is secured in place between an active surface of said die and the first surface of said substrate.

Other features of the present invention are disclosed or made apparent in the section entitled "DETAILED DESCRIPTION OF THE INVENTION".

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the present invention, reference is made to the accompanying drawings in the following Detailed Description of the Invention. Reference numbers and letters refer to the same or equivalent parts of the invention throughout the several figures of the drawings. In the drawings:

FIG. 1 is a cross-section view of a first embodiment of a thermal measuring device constructed in accordance with the principles of the present invention.

FIG. 2 is a flowchart showing a method of constructing a device of the present invention.

FIG. 3 cross-section view of a device as shown in FIG. 1, as clamped during assembly.

FIG. 4 is a cross-section view of another embodiment of a thermal measuring device constructed in accordance with the principles of the present invention.

FIG. 5 is a flowchart showing a method of constructing said another embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The present invention more accurately measures the temperature at the interface between a flip-chip and a packaging substrate during chip attachment to the substrate. By more accurately measuring this temperature, the temperature in reflow furnaces may be adjusted to more accurately optimize process conditions, thereby improving the quality of the solder bond between the chip ("die") and the packaging substrate. This leads to higher circuit reliability and higher process yields.

Referring to FIG. 1, an embodiment illustrating the principles of the present invention is shown. Typically, a flip chip die 1 is provided having an active circuit surface 8 and an inactive surface 7. A typical flip-chip die 1 includes electrically conductive bumps (not shown) formed on the active surface 8. The flip-chip die 1 is positioned top side down (hence the name flip-chip) onto a first side 9 of a packaging substrate 3. The type and size of chip 1 and substrate 3 pair chosen will be similar to those subjected to the reflow process. The idea being that similar chips provide more accurate thermal information. The conductive bumps are aligned with bonding pads formed on the first side 9 of a packaging substrate 3. An interface 6 lies between the die 1 and the first side 9 of a packaging substrate 3. Typically, the height of the solder bumps 2 have been substantially reduced to allow the die 1 to be closer to the first side 9 of a packaging substrate 3. In practice the bump height may be reduced by scraping the bumps using a doctor blade. In the pictured embodiment the bumps have been removed entirely. A thermocouple 5 is positioned between the die 1 and the packaging substrate 3. By way of example, a satisfactory thermocouple 5 is a Model 5TC-GG-K-30-6 thermocouple manufactured by Omega Engineering, Inc. of Stamford Connecticut.

With reference to FIG. 2, such a device may be constructed in accordance with the principles of the present invention by the following method. In Step 201, a semiconductor die is provided. Typically, the die will feature an active circuit surface with electrically conductive bumps for electrically connecting to other circuit elements or the bonding pads of a substrate. The bumps are then removed (Step 202) from the active circuit surface of the die. For example by using a doctor blade to scrape the bumps off. This reduces the distance between the semiconductor die and a subsequently provided packaging substrate. A packaging substrate and a thermocouple are then provided (Steps 203, 204), where the packaging substrate typically includes at least one bonding pad on a first surface. Next, the thermocouple is secured between the active surface of the die and the first side of the packaging substrate (Step 205). A method of satisfactorily securing the thermocouple in place is by treating the thermocouple with an adhesive, typically an epoxy, then contacted the thermocouple to the die. The epoxy treated thermocouple and die are then contacted to the first side of a packaging substrate such that the thermocouple is positioned between the active surface of the die and first side of a packaging substrate.

The thermocouple, substrate, and the die are then clamped (Step 209) together. With reference to Fig. 3, one satisfactory method of clamping the thermocouple 5, the packaging substrate 3, and die 1 together proceeds as follows. A stiffener 20 sized to fit around the die 1 is provided. The stiffener 20 includes a passage 21 enabling the thermocouple 5 to pass through the stiffener 20 once it is placed on the packaging substrate 3. The passage 21 may be a notch in the stiffener 20 or a hole through the stiffener 20. The stiffener 20 is positioned around the die 1 and placed on the first side of a packaging substrate with the thermocouple 5 passing through the small opening 21 in the stiffener 20. A heatspreader 22 is then positioned on the stiffener 20 and die 1. The heatspreader 22 is clamped against the packaging substrate 3 such that the stiffener 22 and die 1 are pressed against the packaging substrate 3 holding the thermocouple 5 in place. A simple clamp 23 may be used to clamp the components together. Other suitable methods of holding the components in place may alternatively be used.

The epoxy is then allowed to cure (Step 210). After curing, the heatspreader and the stiffener are removed, leaving the thermocouple mounted between the packaging substrate and

die. In optional Step 211, the apparatus can be made more robust by soldering the die to the packaging substrate.

FIG. 4 depicts another embodiment of the apparatus of the present invention. The device is comprised of a packaging substrate 3 having a first surface 9 and a second opposite surface 10. The first surface 9 of the packaging substrate 3 typically includes a plurality of bonding pads. A semiconductor die 1 is provided, including a plurality of conductive bumps formed on an active surface 8 thereof. Unlike the previously discussed embodiment, the conductive bumps may remain at their full height. The die 1 is positioned and secured to the first surface 9 of the packaging substrate 3 such that the conductive bumps are aligned with corresponding bonding pads of the packaging substrate 3. This can be conveniently accomplished by treating the bumps with flux and aligning them with the bonding pads of the first surface of the packaging substrate and setting the die in place. The flux has enough "tackiness" to adhere the die 1 to the substrate 3. An opening 11 is made in the second surface 10 of the packaging substrate 3. The opening 11 typically passes through the first surface 9. A thermocouple 5 is placed in the opening 11 and contacted to the semiconductor die 1. The thermocouple 5 is typically secured in place using epoxy, but other methods of securing the thermocouple 5 may be used, for example, solder.

A method of constructing such an embodiment is described with respect to FIG 5. To begin, a semiconductor die is provided (Step 501). Typically, the die semiconductor has solder bumps on an active surface. The solder bumps are typically not removed. Next, a packaging substrate, which typically includes one or more bonding pads on a first surface, is provided (Step 502). As above, the particular semiconductor die and packaging substrate chosen are of the same type semiconductor die and substrate that is to be processed in a reflow furnace.

Next, a thermocouple is provided (Step 503) and an opening is formed (Step 504) in a second surface of packaging substrate, opposite a front surface of the packaging substrate. The opening may be formed by drilling, punching, or other similar means. Also the opening may be formed either before or after assembly with the die. In a preferred embodiment he opening passes through the second surface of the packaging substrate and through the first surface of the packaging substrate. The semiconductor die is secured (Step 505) to the packaging substrate, for example, by dipping the active surface of the semiconductor die in

flux, then aligning the semiconductor die over one of the bonding pads and contacting the semiconductor die to the one of the bonding pads. Adhesion provided by the flux is typically sufficient to hold the semiconductor die to the packaging substrate. Optionally, in Step 506, a stronger bond can be formed between the semiconductor die and the packaging substrate. This is typically accomplished by heating the packaging substrate and the semiconductor die, allowing the solder bumps to reflow and then cool, creating a strong solder bond between the bonding pad and the semiconductor die.

It is contemplated by the inventors that the opening need not be formed prior to the bonding of the semiconductor die to the packaging substrate. The opening may be formed after the semiconductor die has been bonded to the substrate.

Next, the thermocouple is urged (Step 507) into contact with the active surface of the semiconductor die by inserting the thermocouple into the opening. After the thermocouple has been fitted snugly into the opening into position at the interface between the semiconductor die and the packaging substrate, it is cemented (Step 508) into place using an adhesive. Typically, the adhesive will be an epoxy such as FP 454 manufactured by Dexter Electronic Materials of The City of Industry, California. Finally, as needed, the adhesive is cured (Step 509).

The present invention has been particularly shown and described with respect to certain preferred embodiments and features thereof. It is to be understood that the shown embodiments are the presently preferred embodiments of the present invention and as such are representative of the subject matter broadly contemplated by the present invention. The scope of the invention fully encompasses other embodiments which may become obvious to those skilled in the art, and are accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly stated, but rather "one or more". All structural and functional equivalents of the elements of the above-described preferred embodiment that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public

regardless of whether the element, component, or method step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. § 112, paragraph 6, unless the element is expressly recited using the phrase "means for".

CLAIMS

What is claimed is:

1. A device for obtaining an accurate thermal profile of a semiconductor device during processing, said device comprising:

a packaging substrate;

a semiconductor die being positioned on said packaging substrate; and

a thermocouple positioned between said substrate and said die.

2. A device as in Claim 1, wherein said thermocouple is secured in place between said substrate and said die using an adhesive.

3. A device as in Claim 2, wherein said adhesive comprises an epoxy.

4. A device as in Clam 1 wherein said semiconductor die includes an active circuit surface having electrically conductive bumps formed thereon and said packaging substrate includes a plurality bonding pads formed on a surface thereof, said semiconductor die being positioned on said packaging substrate such that said electrically conductive bumps are in electrical contact with said plurality bonding pads.

5. A device as in Claim 4, wherein said packaging substrate and said semiconductor die are secured in place by a solder bond between said electrically conductive bumps and said plurality of bonding pads, said bond securing said thermocouple in position between said packaging substrate and said semiconductor die.

6. A device for obtaining an accurate thermal profile of a semiconductor device during processing, said device comprising:

a packaging substrate having a first surface and a second opposite surface;

said first surface including at least one bonding pad;

a semiconductor die being secured to said at least one bonding pad;

said packaging substrate having an opening in said second opposite surface; and

a thermocouple positioned inside said opening and secured in place.

7. A device as in Claim 6, wherein said opening in said second opposite surface passes through said first surface and said bonding pad.

8. A method of constructing a device for accurately measuring the temperature of a semiconductor device at an interface between a semiconductor die and a packaging substrate, the method comprising the steps of:

a. providing a semiconductor die, said die including an active circuit surface having electrically conductive bumps formed thereon;

b. removing said bumps from said semiconductor die;

c. providing a packaging substrate, said substrate including a first surface for receiving said semiconductor die and an opposite second side;

d. providing a thermocouple; and

e. securing the active surface of said die to the first surface of said substrate such that said thermocouple is positioned between the active surface of said die and the first surface of said substrate.

9. A method as in Claim 8, wherein said step e), of securing said thermocouple between said die and said first surface, includes the steps of:

i) treating said thermocouple with epoxy;

ii) contacting the epoxy treated thermocouple to the active surface of said die;

iii) contacting the epoxy treated thermocouple and the active surface of said die to the first surface of said substrate such that said thermocouple is positioned between the active surface of said die and the first surface of said substrate;

iv) clamping said thermocouple in place between the active surface of said die and the bonding pad;

v) curing the epoxy; and

vi) securing said die, said thermocouple, and said substrate in place by soldering said die to said substrate.

10. A method as in Claim 9, wherein said step iv), of clamping said thermocouple between said die and said first surface of said packaging substrate, includes the steps of:

A. providing a stiffener sized to securely fit around said die, said stiffener including a passage sized to pass said thermocouple through said passage;

B. positioning said stiffener on said first surface of said packaging substrate such that the stiffener fits around said die and allows said thermocouple to fit through the passage;

C. providing a heat spreader;

D. clamping said heat spreader in position on said stiffener such that said die, said stiffener, and said thermocouple are all held in place while said epoxy cures; and

E. after curing the epoxy, removing the heat spreader and the stiffener, leaving the thermocouple epoxied in place between the substrate and die.

11. A method as in Claim 8, wherein said step e), of securing said thermocouple between said die and said first surface of the packaging substrate, includes the steps of:

i) placing said die on the first surface of said substrate such that the electrically conductive bumps of said die are in contact with a plurality of bonding pads formed on said first surface of said substrate; and

ii) reflowing said electrically conductive bumps such that said bumps are secured to said plurality of bonding pads of said substrate to secure said die in place;

iii) forming an opening in said second side of said substrate, said opening passing through said substrate enabling contact with the active circuit surface of said die;

iv) urging said thermocouple into contact with the active surface of said die by inserting said thermocouple into said opening;

v) filling said opening with an epoxy to secure said thermocouple; and

vi) curing the epoxy.

METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

ABSTRACT OF THE DISCLOSURE

A thermal measurement device for obtaining accurate thermal profiles during flip-chip semiconductor packaging and methodologies for making such devices is disclosed. Particularly, a measurement device comprised of a thermocouple sandwiched between a semiconductor packaging substrate and a semiconductor die. Such a device providing increased accuracy in temperature measurement. The present invention also teaches a packaging substrate assembled with a semiconductor die having an opening in the substrate enabling the placement of a thermocouple such that it is in contact with the die and secured in place. Additionally, methods of constructing the devices of the present invention are disclosed.

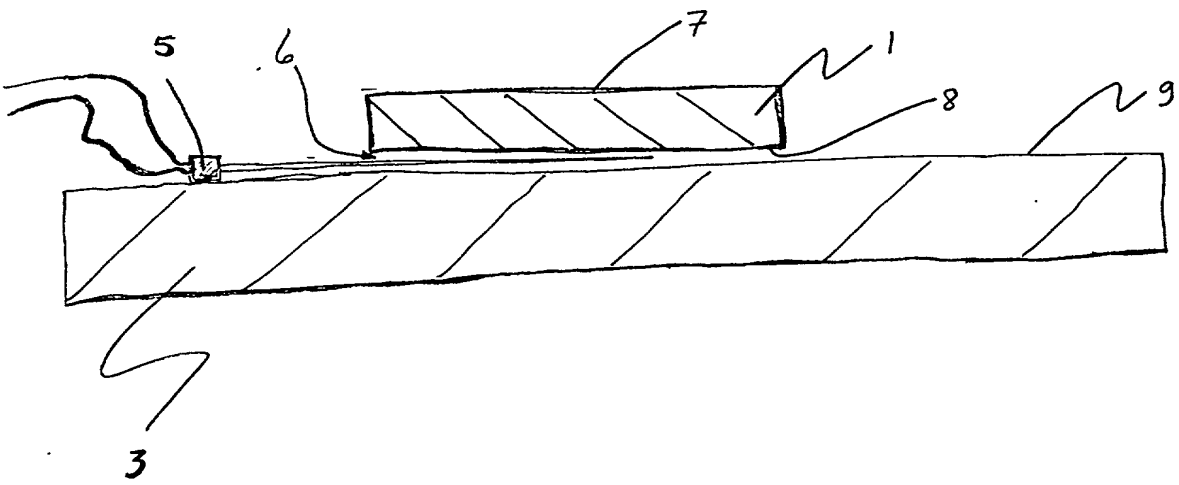

Fig. 1

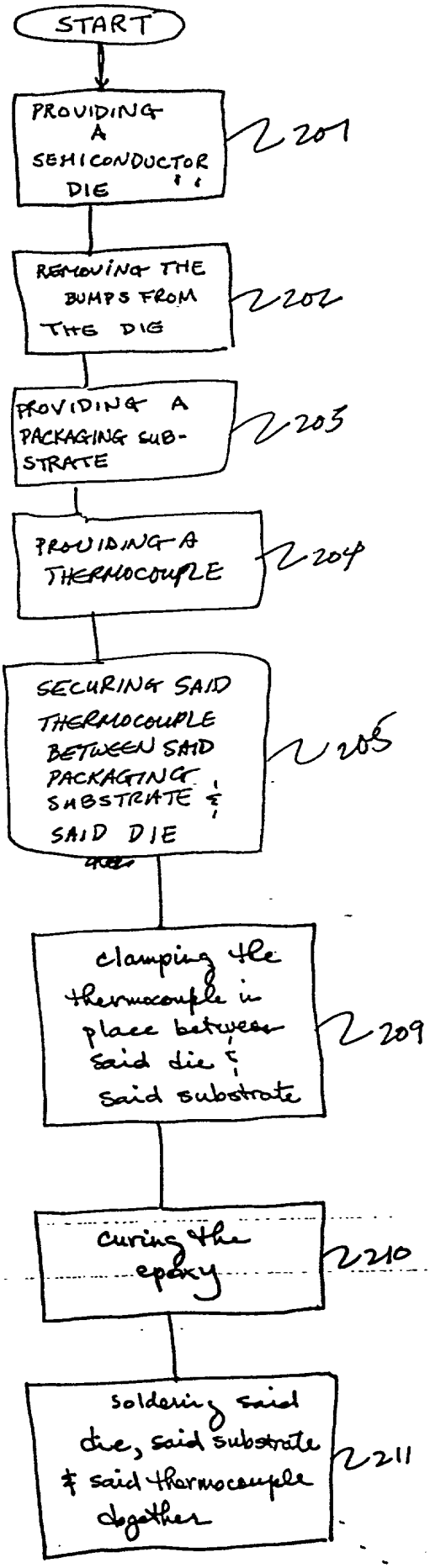

Fig. 2

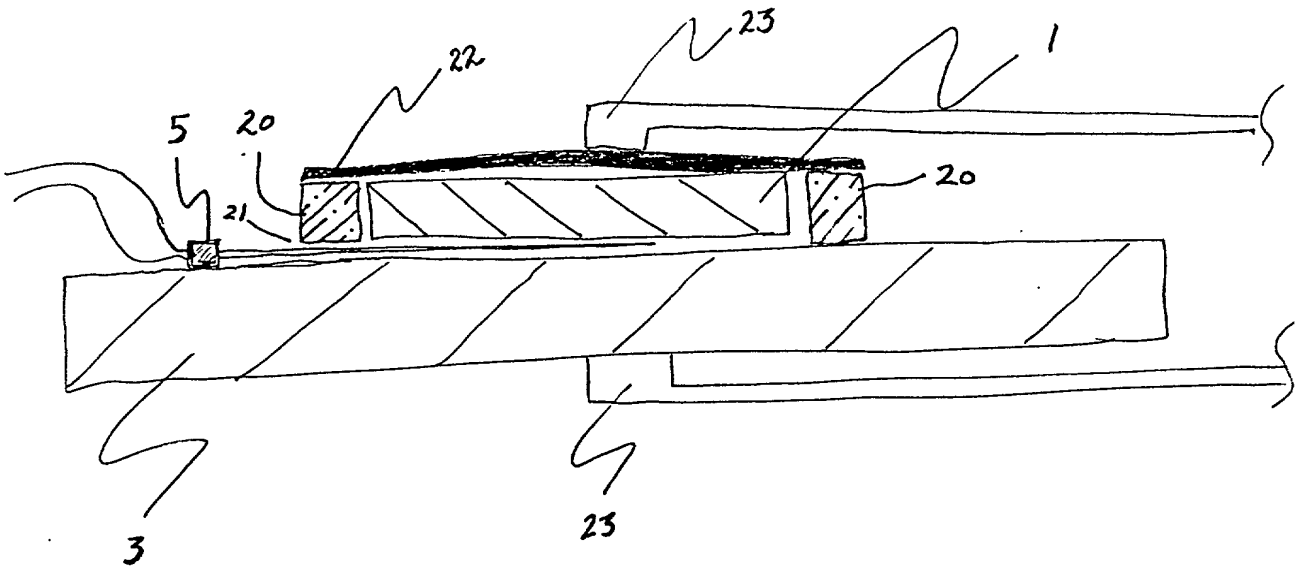

Fig. 3

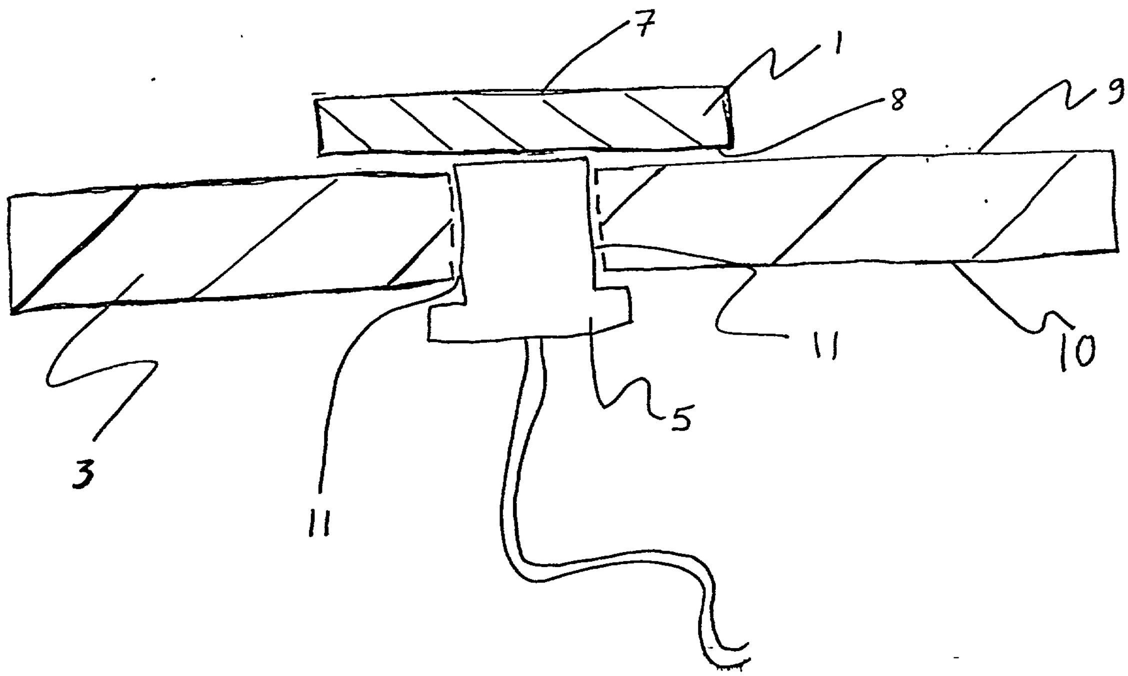

Fig. 4

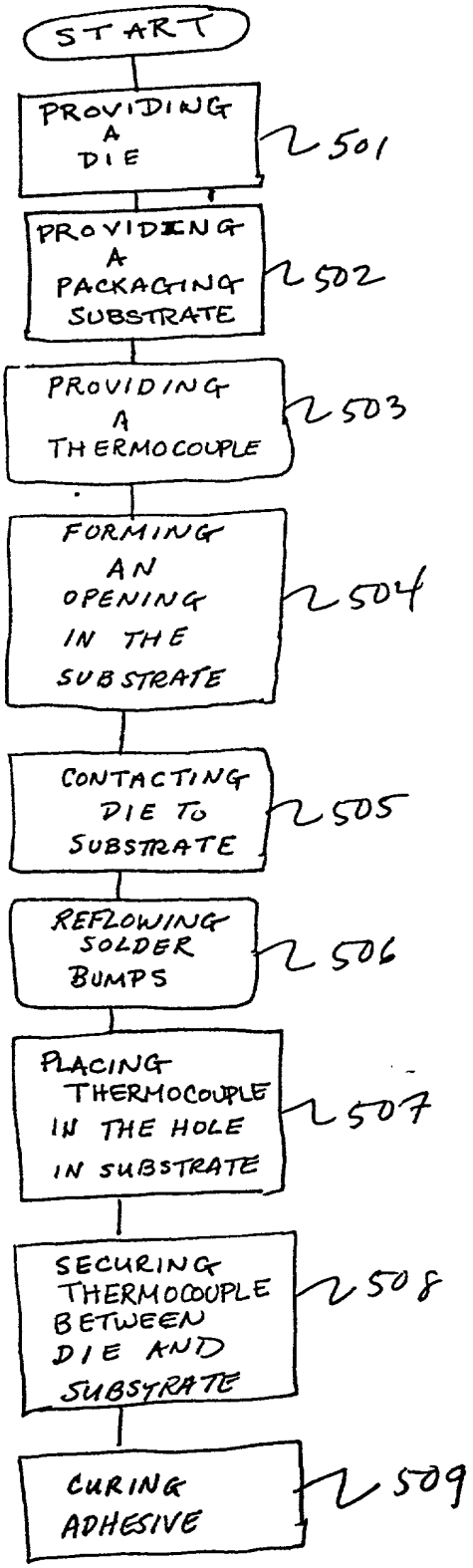

Fig 5

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION		Attorney Docket No.: DOCKET 65611 (P 6653)
		First Named Inventor: Rajagopalan, et al.
[X]Declaration Submitted With Initial Filing	[]Declaration Submitted After Initial Filing	Application Number: TBD Filing Date: Herewith Group Art Unit: Examiner Name:

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

the specification of which:

[x] is attached hereto, or

[] was filed by an authorized person on my behalf on _____ (Date) as United States Application Number or PCT International Application Number _____, and was amended on _____ (Date) (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and I have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application, on this invention filed by me or my legal representatives or assigns and having a filing date before that of the application on which priority is claimed:

Prior Foreign Application Number(s)	Country	Foreign Filing Date	Priority Not Claimed	Certified Copy Attached Yes	Certified Copy Attached No
N/A					

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

Provisional Application Number(s)	Provisional Application Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, §120, of any prior United States application(s), or under §365(c) of any PCT international application(s) designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information known by me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Prior U.S. Application Number	Prior PCT International Application Number	Filing Date of U.S. or PCT International Application	Patent Number (if applicable)
N/A			

As a named inventor, I hereby appoint the following registered practitioners, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, and request that all correspondence and telephone calls in respect to this application be directed to:

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Julius Tabin	16,754	Karl R. Fink	34,161
John F. Flannery	19,759	Thomas F. Lebens	38,221
Robert B. Jones	20,135	Donald A. Peterson	18,647
James J. Schumann	20,856	Bruce R. Mansfield	29,086
James J. Hamill	19,958	Scott J. Menghini	42,880
Timothy E. Levstik	30,192	Francis T. Kalinski	44,177
Joseph E. Shipley	31,137	David G. Pursel	28,659
Robert J. Fox	27,635	Ralph R. Veseli	33,807
Kenneth H. Samples	25,747	Bruce R. Hopenfeld	39,714
Philip T. Petti	31,651	Sandeep Jaggi	43,331

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity or enforceability of the application or any patent issued thereon.

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(Given names first, with Family name last)

Inventor's signature: R P Sarathy

Date: December 15, 1999

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Citizenship: India

Full name of sole or one joint inventor:	Minh Vuong (Given names first, with Family name last)
Inventor's signature:	
Date:	Dec. 15, 1999
Residence:	San Jose, California (City and State for U.S. Residents; City and Country for others)
Post Office Address:	2038 Pollen Court San Jose, CA 95131
Citizenship:	U.S.A.